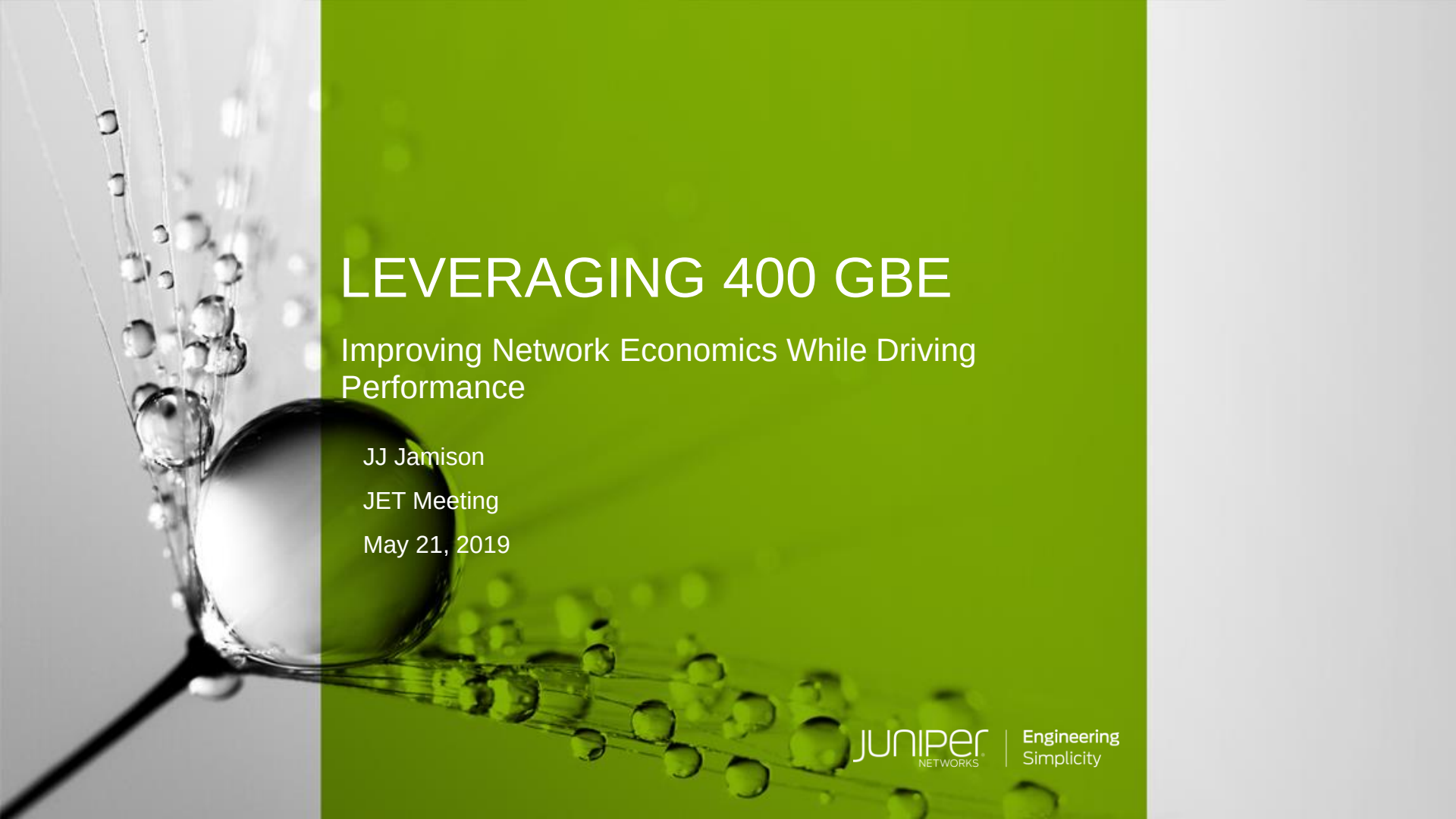




LEVERAGING 400 GBE

Improving Network Economics While Driving
Performance

JJ Jamison

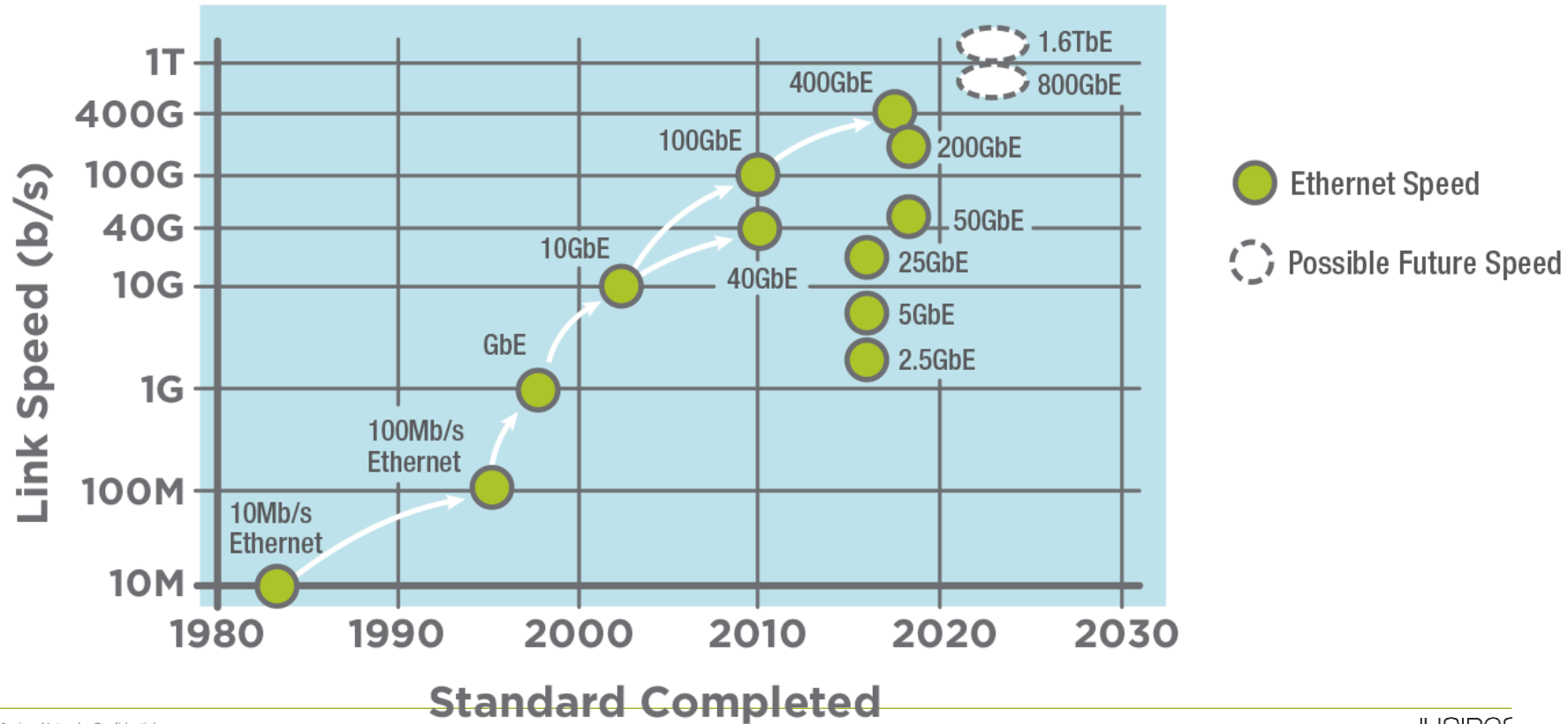
JET Meeting

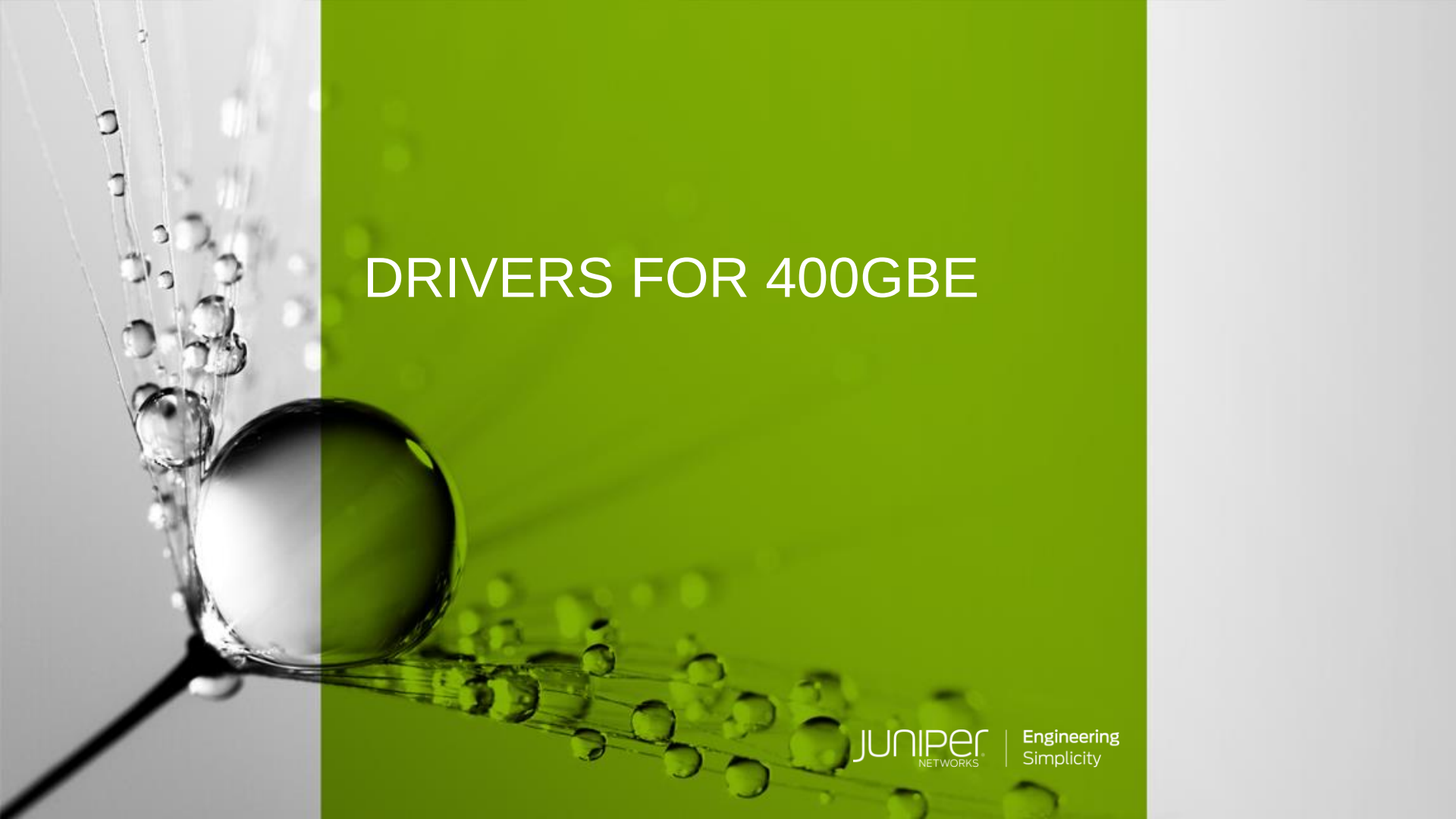
May 21, 2019

JUNIPER
NETWORKS

Engineering
Simplicity

ETHERNET SPEEDS





DRIVERS FOR 400GBE

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WHAT DRIVES JUNIPER'S SOLUTIONS FOR R&E NETWORKS?

The drivers for the solutions we position, and I evangelize, for R&E networks come from other markets.

- Fast/Reliable/Low Cost Routers (Carriers)*

- IPv6 (Carriers)

- Multicast (Wall Street)

- Express Path on Firewalls (Wall Street)

- perfSONAR (read 3rd party apps) on routers and switches (Social Media)

- Node Slicing in R&E Peering Points (Carriers)

400 GE for R&E Networks (Datacenters)

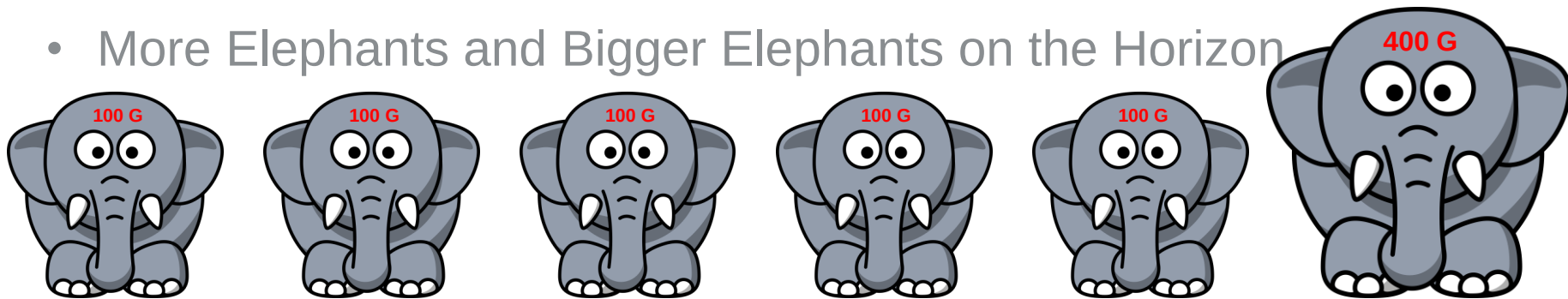
TRENDS DRIVING 400 GE UPTAKE IN DATA CENTERS

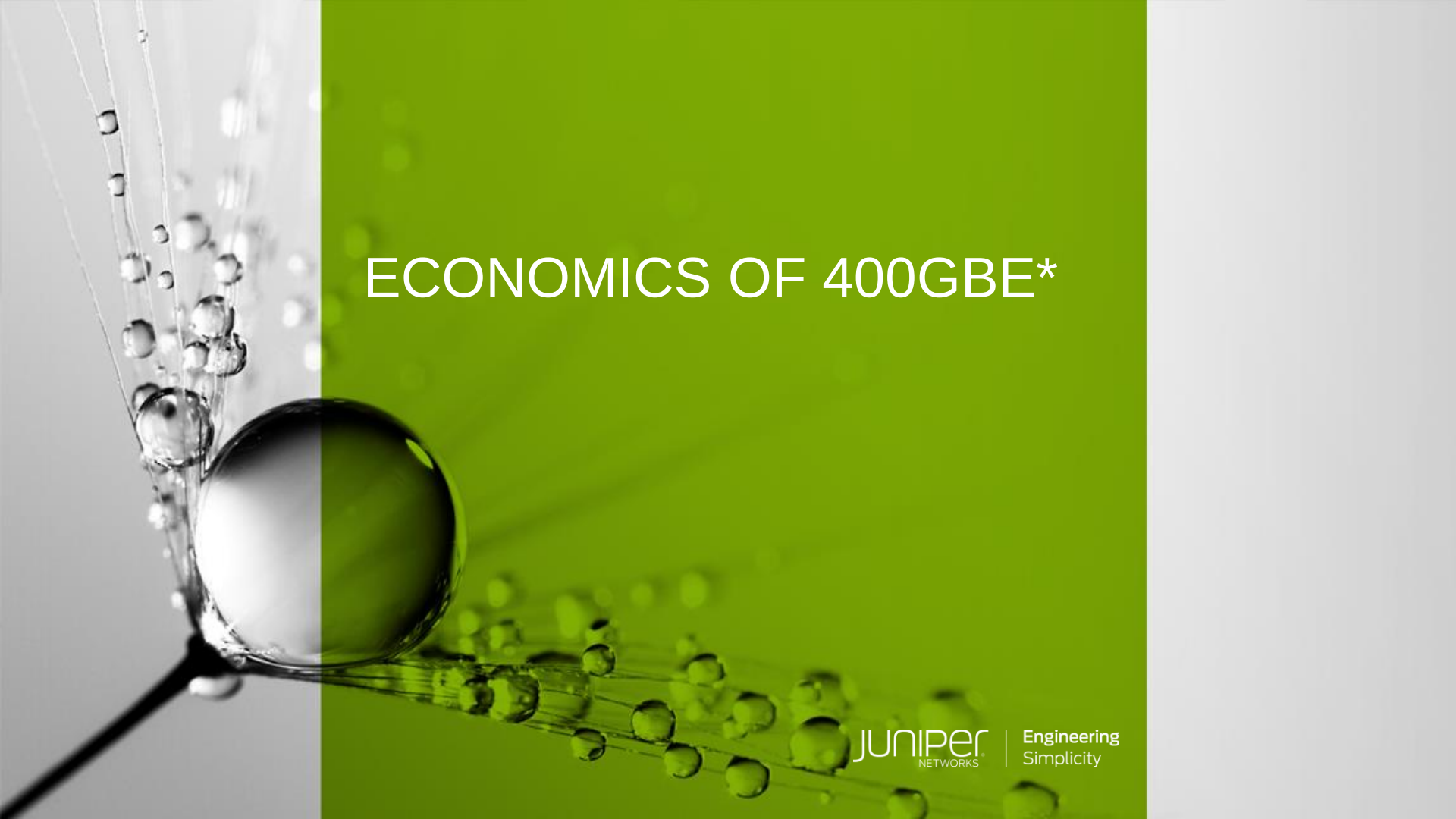
- High Compute Intensive Applications to be run extremely fast on parallel clusters
- Proliferation of Devices resulting in exponential growth of internet data traffic
- Enterprise workloads (Compute and Collaboration)
- Consumer workloads (Video Streaming and Social Networking)
- Digital Transformation of businesses across the entire global spectrum
- Data Center Applications Requirements of HyperScalars:
 - Facebook relies on improved User Experience in spite of ever-growing traffic
 - Amazon relies on Cost control – Minimum Cost incurred per Gigabyte of internet traffic
 - Google, Baidu, Alibaba and Tencent – All rely on Faster Response to queries

Rapid Adoption Forecast: A Dell' Oro Research Report forecasts 400G to comprise 20% of data-center switching revenue by 2020*

TRENDS THAT WILL BE DRIVING 400GE UPTAKE IN R&E

- Elephant Flows
- Massive instruments dumping ridiculous amounts of data where the preference is not to process locally*
- Massive instruments dumping ridiculous amounts of data that is too expensive to process locally
- Proliferation of Science DMZs and DTNs
- More Elephants and Bigger Elephants on the Horizon





ECONOMICS OF 400GBE*

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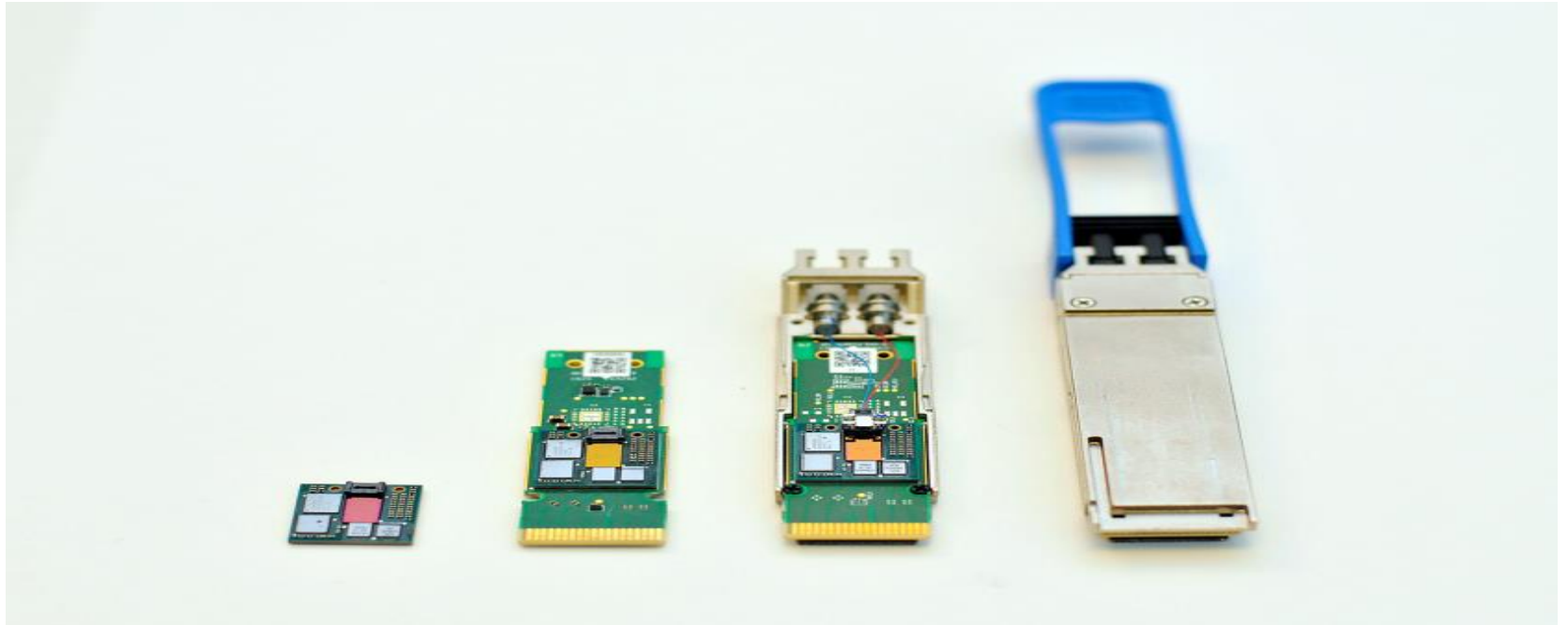
WITH OPTICS ECONOMIES OF SCALE ARE NOT COMPELLING

- Traditionally, Costs of Optical Transceivers driven down solely by Volume Economies of Scale. Suppliers Depend on Demand for more optics to drive down costs.
- In contrast, 100 times larger silicon chip supply chain benefited from shared
 - design methodologies
 - automated wafer manufacturing
 - shared packaging approaches
 - common test infrastructureto deliver unparalleled economies of scale for computing and networking equipment. (Moore's Law)
- Juniper has been successful in lowering cost per bit of its own product portfolio, but dependent on vendors to lower cost of optical interconnects.
- So Juniper acquired Aurion Inc. in 2016 to build in-house silicon photonics technology.

SILICON PHOTONICS

- Silicon photonics leverages benefits of silicon chip ecosystem:
 - Shared design methodologies
 - Outsourced wafer manufacturing to achieve economies-of-scale.
- **Juniper's Differentiation:**
 - Integration of all photonic elements of an optical transceiver— lasers, detectors etc. — within a single silicon photonics die.
 - Integrating Indium phosphide materials into a silicon process flow right on the silicon wafer gives us the ability to amplify or generate light on chip.
 - The ability to incorporate all optical components within a single, common silicon die fundamentally changes and simplifies how an optical transceiver can be assembled and tested, dramatically reducing costs.

“OPTO-ASIC”



Juniper Networks' silicon photonics enabled "Opto-ASIC," a fully integrated transceiver package (left), surface mounted to module board (center left), board assembly placed within module housing with fiber attached (center right), and final QSFP module assembly (right).

“OPTO-ASIC” FUTURES

- Juniper’s fully integrated “Opto-ASIC” transceiver
 - densely packages electronic and photonic die in a single, low-cost package
 - completely agnostic to being packaged in existing module form factors (QSFP, QSFP-DD, OSFP, COBO, etc.)
- Network processors (PFEs: Packet Forwarding Engines)
 - Packet Processing capabilities keep increasing exponentially
 - But, are limited by ability to push that much bandwidth in and out of them electrically – **Shannon’s Law***
 - **Throughput Increase – Possible by integrating photonics & network processor on one Package**
- Juniper’s Silicon Photonics technology offers immense potential:-
 - **Integration into the PFE**, along with Penta Silicon and Triton Silicon, improves scaling performance at the line card and system level, to enable petabit-per-sec total system capacity
 - Combining silicon photonics technology with network processors increases system level capacity and performance while decreasing power consumption

* **Shannon's law:** defines the theoretical maximum rate at which error-free digits can be transmitted over a bandwidth-limited channel in the presence of



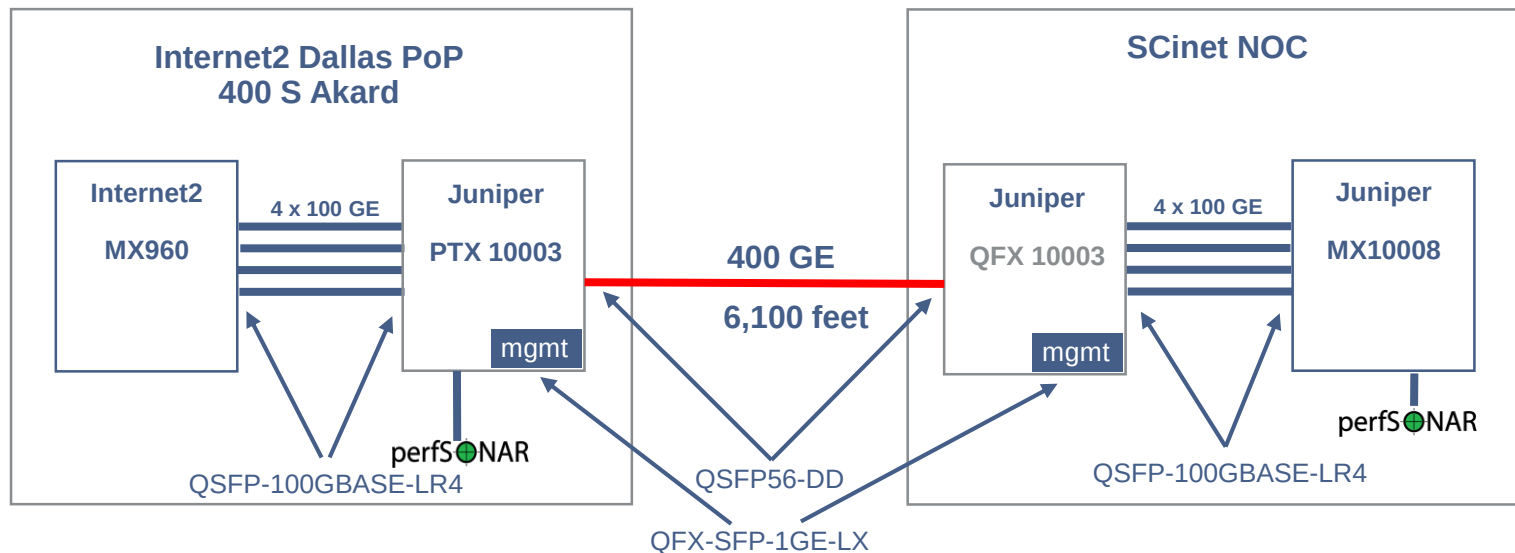
400GBE IN R&E (SO FAR)

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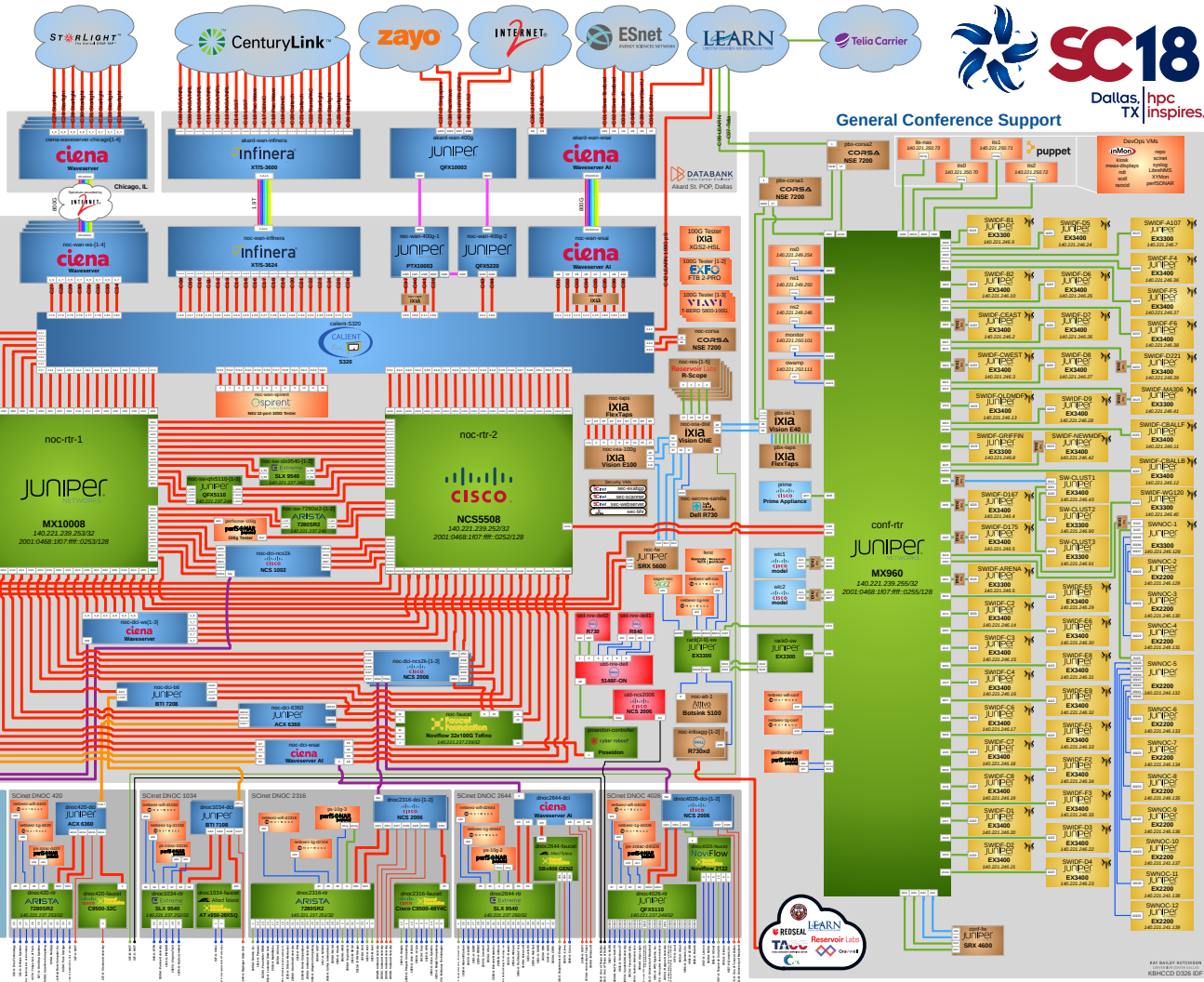
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JUNIPER 400 GE @ SC18

— 100 GE
— 400GE



- 1 Gigabit Ethernet
- 10 Gigabit Ethernet
- 40 Gigabit Ethernet
- 100 Gigabit Ethernet
- 400 Gigabit Ethernet
- 400G DCI
- 800G DCI
- DWDM OTN
- Wi-Fi Access Point



400 GE UPTAKE IN R&E NETWORKS IN 2019

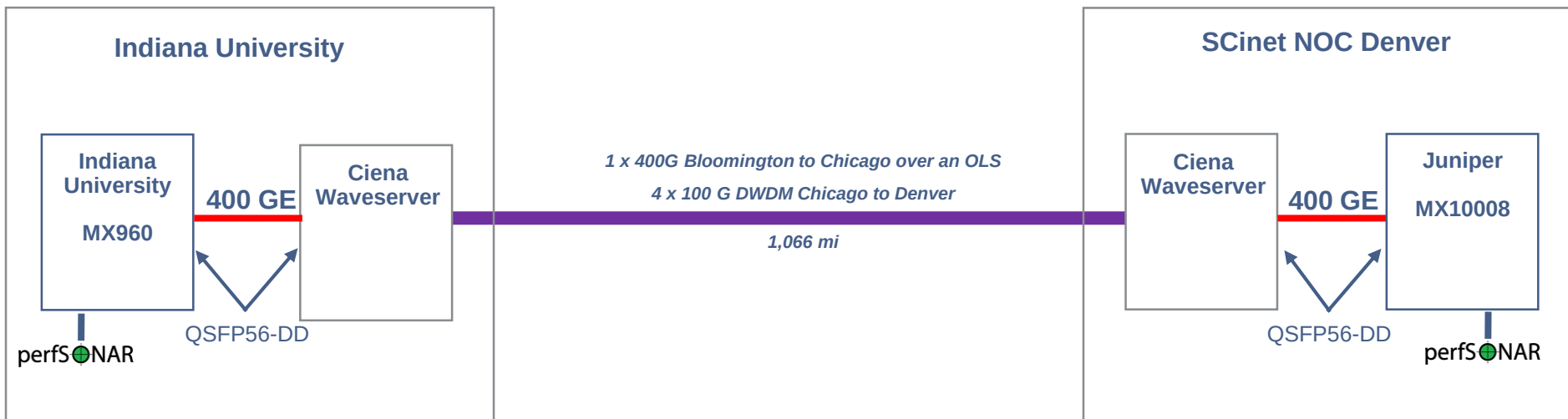
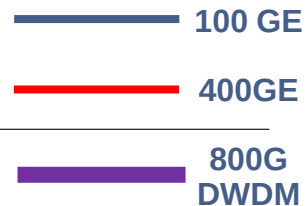
Juniper Account Teams and PLM have had conversations about 400 GE 2019 deployments with:

- A major Supercomputer Center
- Research universities planning on upgrading their WAN access
- Research universities planning 400 GE Science DMZs

We also have had early 400 GE planning conversations with several R&E Network providers

400 GE is coming to R&E Networks this year!

PLANS FOR 2 X 400 GE @ SC19*



The background of the slide features several fingerprints. A solid green vertical bar runs down the center. On either side of this bar, there are grayscale images of fingerprints. One fingerprint is clearly visible on the left, and another is on the right. The text 'THANK YOU / QUESTIONS?' is centered over the green bar in a white, sans-serif font.

THANK YOU /
QUESTIONS?

"Any opinions, findings, conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the Networking and Information Technology Research and Development Program."

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